REMARKS

Claims 1-31 remain pending in this case. In the amendment hereinabove, claims 11, 15, 22 and 24 have been amended to correct typographical errors and lack of antecedent basis. No new matter has been introduced. Based upon the following remarks, it is respectfully submitted that these claims are allowable and this application is in condition for allowance.

A. Claim Objections

Claim 11 was objected to because of an informality; namely, it was noted that the limitation "signal delay circuitry, coupled to said high pass filter circuit, delays . . ." should read "signal delay circuitry, coupled to said high pass filter circuit, that delays . . . ." This correction has been made by way of amendment, and as such, it is submitted that claim 11 is in condition for allowance.

B. Nonstatutory Double Patenting Rejection – *Yu et al. & Hariharan et al.*

Claims 1-8, 15-21 and 24-29 were rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-32 of Yu et al., U.S. Patent No. 6,922,440 ("*Yu et al.*") in view of Hariharan et al., U.S. Patent No. 4,970,703 ("*Hariharan et al.*"). This rejection is respectfully traversed and it is submitted that these claims are in condition for allowance in view of the deficiencies of *Hariharan et al.*

As to claim 1, the Office Action cites column 2, lines 9-11 of *Hariharan et al.* as teaching phase detection circuitry having a selected signal delay. The Office Action asserts that the cited portion of *Hariharan et al.* teaches "providing time delay for two stages" and that "the time delay is interpreted to be the selected signal delay." (Office Action, page 4.) Claim 1, however, requires phase detection circuitry having a selected signal delay. It is respectfully submitted that the Office Action appears to have overlooked this requirement by focusing merely on an alleged

teaching of "providing time delay for two stages" (Office Action, page 4), and that *Hariharan et al.* appears wholly silent as to phase detection circuitry. *Hariharan et al.* is directed to switched capacitor waveform processing circuitry for beam steering applications, wherein each of multiple series-connected stages weights and time delays a signal passing therethrough. (*Hariharan et al.* Abstract.) In particular, the time delays are provided by solid state switches which are closed by switching pulses. (*Hariharan et al.* Abstract and column 2, lines 3-10.) Applicants are unable to find any teaching in *Hariharan et al.* of phase detection circuitry having a selected signal delay.

Further as to claim 1, the Office Action cites column 2, lines 12-14 as teaching that the selected signal delay is selected such that an integrated signal provided from signal integration circuitry has a substantially zero AC signal component. However, it is respectfully submitted that the cited portion of *Hariharan et al.* teaches that the output of each delay stage amplifier, not an integrated signal, is placed at AC zero through discharge of a feedback capacitor by a pulse Q_3, not by particular selection of a selected signal delay. Indeed, pulse Q_3 is unrelated to *Hariharan et al.*'s time delays, which are controlled by pulses Q_1 and Q_2. (*Hariharan et al.* column 2, lines 10-11.)

In view of the aforementioned deficiencies of *Hariharan et al.*, it is submitted that the Office Action has not established a prima facie case of obviousness with respect to claim 1, and that claim 1 is therefore in condition for allowance. Therefore, it is further submitted that the Office Action has not established a prima facie case of obviousness with respect to dependent and multiple dependent claims 2-8, and that claims 2-8 are therefore in condition for allowance as well, particularly in view of these claims' further limitations.

As to claims 15 and 24, it is noted that these claims contain the same or similar limitations as found in claim 1. Accordingly, the relevant remarks set forth above as to the

deficiencies of *Hariharan et al.* with regard to claim 1 are respectfully reasserted. For at least the reasons set forth in those remarks, it is submitted that the Office Action has not established a prima facie case of obviousness with respect to claims 15 and 24, and that claims 15 and 24 are therefore in condition for allowance. Therefore, it is further submitted that the Office Action has not established a prima facie case of obviousness with respect to these claims' dependent and multiple dependent claims 16-21 (which depend from claim 15) and 25-29 (which depend from claim 24). Accordingly, it is submitted that claims 16-21 and 25-29 are in condition for allowance as well, particularly in view of these claims' further limitations.

C. § 112 Rejection

Claims 15 and 24 were rejected under 35 U.S.C. § 112, second paragraph, as lacking sufficient antecedent basis. Specifically, it was noted that the limitation "said selected delay signal" in each of these claims had insufficient antecedent basis. It is noted that these claims do not contain the limitation "said selected delay signal", but do contain the limitation "said selected signal delay"; therefore, it is believed that the former was a typographical error and this rejection has been addressed accordingly. Claims 15 and 24 have each been amended to add limitations establishing antecedent basis for the limitation "said selected signal delay". No new matter is believed to have been added by these amendments, which find full support at, for example, page 10, lines 18-30 of the present disclosure. As such, it is submitted that claims 15 and 24 are in condition for allowance.

D. § 102(b) Rejection – *Choi*

Claims 1, 9, 12, 14-15, 22-24 and 30-31 were rejected under 35 U.S.C. § 102(b) as being anticipated by Choi, U.S. Patent No. 6,201,832 (*"Choi"*). This rejection is respectfully traversed and it is submitted that these claims are patentable over *Choi*.

Choi is directed to a synchronous/asynchronous data detection apparatus for use in a magnetic recording/playback system. (*Choi* Abstract.) The data detection apparatus includes an equalization channel. (*Choi* column 5, line 13.) As an initial matter, however, it is noted that the adaptive equalization channel taught by *Choi* lacks anything equivalent to the adaptive timing control block of the present invention. As noted in the present disclosure, the claimed adaptive timing control block processes a feedback error signal and a pre-decision data signal to produce an adaptive signal for the combining circuit denoted by reference numeral 18. (Present disclosure, page 9, lines 6–9.) Assuming solely for the sake of argument that *Choi* teaches a circuit corresponding to the combining circuit of the present invention, the closest such teaching appears to be that of the subtractor denoted by reference numeral 55, which subtracts an output signal of a decision circuit from an *i*th equalized sample value ES_i. (*Choi*, column 14, lines 41–45 and FIG. 2.) This subtractor, in turn, does not receive any inputs from circuitry that processes a feedback error signal and a pre-decision data signal to produce an adaptive signal. Instead, the subtractor receives its inputs from a feedforward equalization circuit and a decision feedback equalization circuit (*Choi*, FIG. 2). These components may also be present in a system employing the presently claimed adaptive timing control block (present disclosure, page 2, lines 20-27), *i.e.*, *in addition to* the claimed adaptive timing control block itself.

Specifically as to claim 1, it is submitted that *Choi* fails to teach, among other things, interpolating mixer circuitry that receives and mixes an integrated signal and a pre-decision data signal to provide an adaptive signal. The Office Action has cited the "interpolation filter 20" of *Choi* as teaching the claimed interpolating mixer circuitry. It is respectfully submitted, however, that *Choi* does not teach an interpolation filter that receives either of an integrated signal or a pre-decision data signal. Rather, the interpolation filter of *Choi* receives: (1) a phase error signal

PE_{i-1} from a loop filter and (2) an *i*th sample value S_i from an analog-to-digital converter. For the reasons set forth in detail hereinafter at page 18, second full paragraph, it is submitted that the phase error signal PE_{i-1} received from the loop filter is not an integrated signal. Likewise, the *i*th sample value S_i from the analog-to-digital converter is not a pre-decision data signal. Specifically, in the present disclosure, the pre-decision data signal is indicated by reference numeral 13/23 (Present disclosure, page 2, line 30); that is, in the present disclosure, the pre-decision data signal is an initially equalized signal (13) provided by a feedforward filter or, in a system employing decision feedback equalization, is the sum (23) of the initially equalized signal (13) and an equalized signal (21) provided by a feedback filter (Present disclosure, page 2, lines 20–27 and FIG. 1). The *i*th sample value S_i in the apparatus of *Choi*, by contrast, is merely an output provided by an analog-to-digital converter, before any feedforward or feedback filtering occurs. (*Choi*, FIG. 2.) In fact, even assuming for the sake of argument that *Choi* does teach a signal corresponding to the claimed pre-decision data signal, the closest such teaching appears to be that of the *i*th equalized sample value ES_i, which is the sum of: (1) first equalized signal provided by a feedforward equalizer (via line L16) and (2) a second equalized signal provided by a feedback equalizer (via line L17). (*Choi*, column 8, lines 20–33 and 64–67.)

Accordingly, it is respectfully submitted that the interpolation filter of *Choi* does not receive either an integrated signal or a pre-decision data signal. It is further submitted that the interpolation filter of *Choi* does not mix the two signals that it does receive, as is further required by claim 1. *Choi* instead teaches that an interpolation filter performs extensive processing on one of the signals it receives, *i.e.*, the phase error signal PE_{i-1}, and then mixes the result of that processing with the other signal it receives, *i.e.*, the *i*th sample value S_i from the analog-to-digital converter. (*Choi*, column 6, line 26 – column 7, line 15.)

Additionally, the signal provided by the interpolation filter is not an adaptive signal, as still further required by claim 1. Rather, the signal provided by the interpolation filter is an *i*th interpolated sample value IS_i which is the input to an adaptive equalization channel and is provided to a feedforward equalizer. (*Choi*, column 5, lines 57–63 and FIG. 2.) In fact, in view of the remarks hereinabove regarding *Choi*'s failure to teach anything equivalent to the adaptive timing control block of the present invention, it is submitted that *Choi* does not appear to teach anything at all equivalent to the claimed adaptive signal.

Simply stated, the interpolation filter of *Choi* is not part of an adaptive timing control block within an adaptive equalizer because *Choi* wholly fails to teach such an adaptive timing control block. As such, it is respectfully submitted that *Choi* fails to teach the claimed interpolating mixer circuitry.

Further as to claim 1, it is respectfully submitted that *Choi* does not teach phase detection circuitry coupled to first and second signal terminals as such signal terminals are defined in claim 1. As set forth in the first two limitations of claim 1, the first and second signal terminals convey, respectively: (1) a pre-decision data signal having a data symbol period associated therewith, and (2) an error signal corresponding to a difference between an adaptive signal and a post-decision data signal. The Office Action has cited the phase error detector (reference numeral 70) of *Choi* as allegedly teaching the claimed phase detection circuitry. The phase error detector, however, is coupled to an (*i*-1)st error signal E_{i-1}, an *i*th decision value D_i, and an (*i*-2)nd decision value D_{i-2}. (*Choi*, column 14, lines 52-55 and FIG. 2.) None of these signals is either a pre-decision data signal or an error signal corresponding to a difference between an adaptive signal and a post-decision data signal. For ease of examination, it is noted that the (*i*-1)st error signal E_{i-1} does not correspond to a difference between an adaptive signal and a post-

decision data signal because of *Choi*'s failure to teach anything equivalent to the claimed adaptive signal, as discussed hereinabove. Indeed, *Choi*'s *i*th error signal E_i corresponds to a difference between an *i*th equalized sample value ES_i and an (*i*-1)st decision value D_{i-1}. (*Choi*, column 14, lines 41–43 and FIG. 2.) As noted hereinabove, *Choi*'s *i*th equalized sample value ES_i appears to correspond, at best, to the pre-decision data signal of the present invention. As such, it is submitted that the (*i*-1)st error signal E_{i-1} appears to correspond, at best, to a difference between a pre-decision data signal and a post-decision data signal.

Further still as to claim 1, it is respectfully submitted that *Choi* does not teach phase detection circuitry having a selected signal delay. The Office Action has cited "the delay from delay circuit 700 in fig. 9" as teaching this limitation. However, the delay circuit taught by *Choi* is not part of the alleged phase detection circuitry (*i.e.*, reference numeral 70), but instead is part of a loop filter (reference numeral 80) which is alleged to teach the signal integration circuitry that is further required by claim 1. It is therefore respectfully submitted that the Office Action's citation of the delay circuit as teaching a limitation pertaining to the claimed phase detection circuitry is improper.

Claim 1 also requires signal integration circuitry, coupled to the phase detection circuitry and the interpolating mixer circuitry, that receives and integrates a detection signal—provided by the phase detection circuitry—to provide an integrated signal. The Office Action has cited the loop filter (reference numeral 80) of *Choi* as teaching this limitation. However, it is respectfully submitted that *Choi* appears silent on any signal integration capability of not only its loop filter, but its entire disclosure. As such, in the event that the rejection is maintained, Applicants respectfully request a specific showing by column and line number of any teaching by *Choi* of signal integration.

Additionally, claim 1 requires that the selected signal delay of the phase detection circuitry is selected such that the integrated signal provided by the signal integration circuitry has a substantially zero AC signal component. The Office Action has cited *Choi*, column 15, lines 31–37 as teaching this limitation, stating that "the predetermined analog voltage level to the VCO circuit is interpreted to be *substantially* zero" (emphasis in original). However, it is respectfully submitted not only that a predetermined analog voltage level is not equivalent to an AC signal component, but also that the cited portion of *Choi* appears completely silent as to any signal with a substantially zero AC signal component. The Office Action has not identified any support for its interpretation of the cited portion as teaching the claimed limitation, and Applicants are unable to locate any such teaching in any portion of *Choi*. As such, it is respectfully submitted that *Choi* fails to teach the claimed limitation. In the event the rejection is maintained, Applicants respectfully request a specific showing by column and line number in *Choi* of any alleged teaching of this limitation.

For all of the above reasons, it is submitted that claim 1 is patentable over *Choi*. Therefore, it is further submitted that its dependent and multiple dependent claims 9, 12 and 14 also recite subject matter which is patentable over this reference as well, particularly in view of these latter claims' further limitations.

As to claims 15 and 24, it is noted that these claims contain the same or similar limitations as found in claim 1. Accordingly, the relevant remarks set forth above as to *Choi*'s failure to teach the limitations of claim 1 are respectfully reasserted. For at least the reasons set forth in those remarks, it is submitted that claims 15 and 24 are patentable over *Choi*. Therefore, it is further submitted that these claims' dependent claims 22–23 (dependent on claim 15) and

30–31 (dependent on claim 24) also recite subject matter which is patentable over this reference as well, particularly in view of these latter claims' further limitations.

E. § 103(a) Rejection – *Choi & Goldston et al.*

Claims 10–11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Choi, U.S. Patent No. 6,201,832 ("*Choi*") in view of Goldston et al., U.S. Patent Application Publication No. 2002/0012392 ("*Goldston et al.*"). This rejection is respectfully traversed and it is submitted that these claims are patentable over *Choi* and *Goldston et al.*

In accordance with and with reference to the remarks in Part D hereinabove, it is submitted that independent claim 1 is patentable over *Choi*, and it is further submitted that this claim is patentable over *Choi* and *Goldston et al.* Therefore, it is still further submitted that multiple dependent claims 10–11 are patentable over *Choi* and *Goldston et al.* as well, particularly in view of these latter claims' further recited limitations.

F. § 103(a) Rejection – *Choi & Copeland*

Claim 13 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Choi, U.S. Patent No. 6,201,832 ("*Choi*") in view of Copeland, U.S. Patent No. 6,067,319 ("*Copeland*"). This rejection is respectfully traversed and it is submitted that this claim is patentable over *Choi* and *Copeland.*

In accordance with and with reference to the remarks in Part D hereinabove, it is submitted that independent claim 1 is patentable over *Choi*, and it is further submitted that this claim is patentable over *Choi* and *Copeland.* Therefore, it is still further submitted that dependent claim 13 is patentable over *Choi* and *Copeland* as well, particularly in view of this latter claim's further recited limitations.

G. Conclusion

Claims 1–31 remain pending in this case. Based upon the foregoing remarks, it is respectfully submitted that these claims are allowable, and reconsideration and early allowance of these claims are requested.

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Respectfully submitted,

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